Notice of Allowability	Application No.	Applicant(s)	
	10/717,040	NGAI ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed 01/30/2007 and arguments/amendments filed 12/21/2006*.

2. ☒ The allowed claim(s) is/are *1-42*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

DETAILED ACTION

1. Claims 1-42 remain pending in the current application. Claims 1, 2, 15, 25 and 34 have been amended.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/30/2007 has been entered.

Response to Arguments

3. Applicant's arguments, filed 12/21/2006, with respect to claims 1-42 have been fully considered and are persuasive. The Final rejection of 10/19/2006 has been withdrawn.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided

by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Lois D. Cartier on 03/01/2007.

The application has been amended as follows:

Claim 1, line 17: Change "the column" to "each column".

Claim 11, line 12: Change "coupled to" to "carried in from", so the line reads "volatile memory circuits, a second input *carried in from* an output of a logic circuit".

Claim 15, line 17: Change "the column" to "each column".

Claim 25, line 16: Change "the column" to "each column"; line 22, change "the first column" to "the first adjacent column".

Claim 34: Delete the "and" and the end of lines 12 and 14; line 19, change "the first column" to "the first adjacent column".

Claim 34: Add the following after line 14: "means for generating for each column of RAM cells a respective selection signal as a function of the error flag associated with each column and a selection signal carried in from an adjacent column of RAM cells; and"

Claim 35: Add the word "and" to the end of line 11, so it reads "the second array; and". Delete lines 12-14, which starts with "generating for each column of RAM cells..." and ends with ";and".

Allowable Subject Matter

5. Claims 1-42 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention relates to Programmable Logic Devices (PLDs). More particularly, the invention relates to a memory block in a PLD that detects and automatically repairs defects during the configuration process for the PLD.

The claimed invention as set forth in independent **claim 1** recites features such as: A method of configuring a programmable logic device (PLD) which comprises a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells;

initiating a configuration sequence for the PLD;

initiating a built in self test (BIST) procedure on the first array;

setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array;

wherein a respective error flag is associated with each column of RAM cells in the first array;

loading first PLD configuration data into the first RAM circuit, wherein when the first error flag is set the first PLD configuration data bypasses the first defective column of the RAM cells and a first portion of the first PLD configuration data is loaded into the first redundant column of the RAM cells; and

wherein the loading comprises generating for each column of RAM cells a respective selection signal as a function of the error flag associated with each column and a selection signal carried in from an adjacent column of RAM cells, and selecting for input to each column of RAM cells in response to the respective selection signal, one of a first set of bits of configuration data addressed to the column of RAM cells and a second set of bits of configuration data addressed to the adjacent column.

The prior arts of record teach the initiating, setting and loading steps as claimed. The prior arts of record discloses when a column of logic blocks is found to be defective, a redundant column is switched into the matrix by decoders, which control bits are reprogrammed to shift the configuration data into the redundant column, effectively bypassing the defective column; **Cliff et al.** (US005498975) and **Rao et al.** (US006055205) are examples of such prior arts. Newly cited prior art **Dixon et al.** (US 20050022065) discloses a bit-swapping circuit 400, which uses a centrally placed spare-bit replacement controller 510.

The prior arts of record, however, fail to teach, singly or in combination, *generating for each column of RAM cells a respective selection signal as a function of the error flag associated with each column and a selection signal carried in from an adjacent column of RAM cells*. The prior arts of record do not show a selection signal carried in from an adjacent column being used to generate the selection signal for the current column. As such, modification of the prior art of record to include the claimed *carried-in selection signal* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that

one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *carried-in selection signal* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *carried-in selection signal* as set forth in **claim 1**. Independent **claims 15, 25 and 34** claims the same *carried-in selection signal* as **claim 1** and are allowable for the same reasons.

The claimed invention as set forth in **claim 11** recites features such as: a programmable logic device (PLD), which comprises a first read/write data access port;

a first random access memory (RAM) circuit comprising a first array of rows and columns of RAM cells and a first redundant column of the RAM cells;

a first routing circuit coupled between the first data access port and the first RAM circuit;

wherein the first routing circuit comprises a plurality of volatile memory circuits, a plurality logic circuits, and a plurality of selector circuits, each volatile memory circuit, logic circuit, and selector circuit respectively associated with one of the columns of RAM cells;

wherein each logic circuit has a first input coupled to a respective one of the volatile memory circuits, a second input *carried in from* an output of a logic circuit associated with an adjacent column of RAM cells, and an output coupled to a selector input of the selector circuit;

wherein each selector circuit selects for input to the associated column of RAM cells, one of a first set of bits of configuration data addressed to the column of RAM cells and a second set of bits of configuration data addressed to the adjacent column;

a built in self test (BIST) control circuit coupled to the volatile memory circuits of the first routing circuit and further coupled to the first RAM circuit;

wherein the BIST control circuit is configured to test whether each column of RAM cells is defective, and responsive to a defective column of RAM cells, store a first value in the volatile memory circuit associated with the defective column of RAM cells;

a configuration data port; and

a configuration control circuit coupled to the BIST control circuit, the configuration data port, and the first RAM circuit.

The prior arts of record substantially teaches the limitations as claimed; The prior arts of record discloses when a column of logic blocks is found to be defective, a redundant column is switched into the matrix by decoders, which control bits are reprogrammed to shift the configuration data into the redundant column, effectively bypassing the defective column; **Cliff et al.** (US005498975) and **Rao et al.** (US006055205) are examples of such prior arts. Newly cited prior art **Dixon et al.** (US 20050022065) discloses a bit-swapping circuit 400, which uses a centrally placed spare-bit replacement controller 510.

The prior arts of record, however, fail to teach, singly or in combination, the claimed *each logic circuit has a first input coupled to a respective one of the volatile*

memory circuits, a second input carried in from an output of a logic circuit associated with an adjacent column of RAM cells, and an output coupled to a selector input of the selector circuit. The claimed *second input of the logic circuit* is the *carried-in selection signal* claimed in **claims 1, 15, 25 and 34**. As such, modification of the prior art of record to include the claimed *second input of the logic circuit* can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior art themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior art of record to encompass the *second input of the logic circuit* set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the *second input of the logic circuit* as set forth in **claim 11**. Hence, **claims 1-42** are allowable over the prior arts of record.

The Examiner agrees with the Applicant's arguments with regard to this feature in view of the arts of record; therefore, the Examiner favors the allowance of claims 1-42. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 2/28/07
Examiner
Art Unit 2138